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A high resolution DDFS design on VHDL using Bipartite Table Method

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ABSTRACT

In this study, a Look Up Table (LUT) based Direct Digital Frequency Synthesizer (DDFS) is designed on VHDL. Bipartite Table Method, an advance memory compression method, is used together with quadratic compression method. 23 mHz frequency resolution is achieved with 100MHz clock input. The required memory is obtained 585 times smaller than traditional DDFSs. A MATLAB code is revealed to select the best design which provides the smallest required memory for 100 dB Spurious Free Dynamic Range (SFDR) level. The contents of the LUTs are also evaluated by using MATLAB software. The design is simulated for multiple frequencies between 23mHz-30MHz with VIVADO 2016.3 software. The simulation results perfectly match with calculations.

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1. Introduction

Frequency synthesizers are the systems that generate signals with new frequencies from one or more reference signal. In the history of frequency synthesizers, several approaches are proposed to synthesize new frequencies and these approaches are divided in three major groups. These are Direct Analog, Direct Digital and Indirect Frequency Synthesizers.

Direct Digital Synthesis is the one which provides fast switching speed, very high frequency resolution, low phase noise, ease to control output frequency precisely and utilized in several areas such as communication [1]-[3] test and measurement systems [4], [5], image processing [6] and medical applications [7].

A typical Direct Digital Frequency Synthesizer (DDFS) uses ROMs as Look Up Tables (LUTs) to convert the phase values to amplitude values. The ROMs contains the digital samples of the desired signal form. A counter is used as a phase accumulator. The phase accumulator controls the frequency of the output signal with a digital Frequency Tuning Word (FTW). The word changes the step size of the address counter of the ROM. Thus, the desired frequency is adjusted digitally. The output frequency is evaluated by the following equation where $\mathrm{f_{clk}}$ is the reference clock signal and 2^{N} is the number of phase values on the counter.

$$\mathrm{f_{out}} = \mathrm{FTW} \times \frac{\mathrm{f_{clk}}}{2^{\mathrm{N}}} \quad (1)$$

A Digital to Analog Converter (DAC) is used to get the analog signal. Principle stages of a DDFS are given in Fig. 1.

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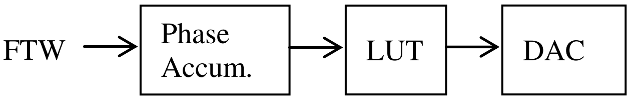


Figure 1. Principal stages of a traditional LUT based DDFS

In DDFS designs, many improvements are revealed to achieve better spectral performance [8], lower power dissipation [9], [10], higher frequency resolution [11] and smaller required area [12]-[14].
This paper presents a high resolution, LUT based DDFS design on VHDL. Bipartite Table Method (BTM) which is offered by Dinechin and Tisserand in 2005 is used to lessen the LUT size while keeping the Spurious Free Dynamic Range (SFDR) above 100 dB.

1.1. LUT Based DDFSs

In DDFS, the phase to amplitude conversion is done in several ways. LUT based [12]-[14],iterative approaches [15] and LUT free approaches [16] are the most common ones of these ways. LUTs are the tables that store the sampled data of a signal form. The size of the LUT determines the resolution and the spectral performance of the signal to be generated. Table 1 shows the content of a 32x8 bits LUT for a sine.

Table 1. Contents of a typical 32x8 bits LUT for a sine

0	49	71	91	106	118	126	128
126	118	106	91	71	49	25	0
-25	-49	-71	-91	-106	-118	-126	-128
-126	-118	-106	-91	-71	-49	-25	0

As shown from the Table 1, the LUT stores 32 digital data represented with 8 bits signed numbers. When a sine is generated from this small LUT, the approximate SFDR value of the generated signal is evaluated as 53.62 dB with the *sfdr (x)* command in MATLAB. Although the spectral performance seems good, the phase and amplitude resolutions are both unsatisfactory. The generated sine is shown in Fig. 2.

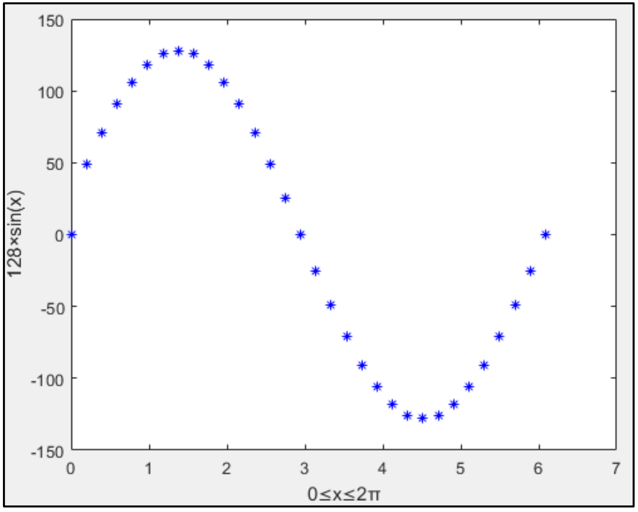


Figure 2. The sine generated from the 32x8 bits LUT

The increase in resolution or spectral performance requires an increase in the LUT size. De Caro and his friends claim that their design requires only 208 bits to provide higher SFDR level with 11 bits phase and 9 bit amplitude resolution. To obtain this much phase and amplitude resolution, a 18,432 bits-LUT is required in a traditional DDFS structure. There are several LUT based studies providing 100 dBc and higher SFDR levels with very high phase and amplitude resolution [14], [17]. The common idea behind these studies is to compress the ROM size as much as possible while keeping the SFDR level and the resolutions good enough. In this design, BTM is used to compress the ROM while keeping the SFDR above the predetermined levels.

2. Method

2.1. Bipartite Table Method (BTM)

In this part of the paper BTM which is the one of the LUT based approaches is introduced.The method uses piecewise linear approach. In this method two different LUT is used. Firstly, 2^a initial values are evaluated and stored in the first LUT. This table is called table of initial values (TIV). Fig. 3 shows the initial values for the one fourth of a sine period for 32 initial values with the 8 bit amplitude resolution (R). The TIV size is calculated as

$$\mathrm{TIV_{size}} = \mathrm{R} \times 2^{\alpha} \tag{2}$$

Secondly, some offset values are evaluated and stored in the second LUT. The table is called as table of offsets (TO). The TO values are calculated by using piecewise linear approach with the following equations.

$$\mathrm{m_i} = \frac{\mathrm{f(x_{i+1}) - f(x_i)}}{\mathrm{x_{i+1} - x_i}} \tag{3}$$

$$\mathrm{f(x) = m_i\,(x - x_i)} \tag{4}$$

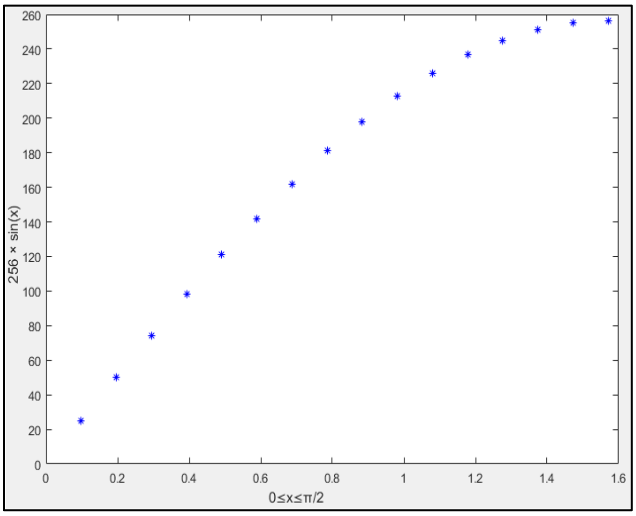


Figure 3. The initial values for the one fourth of sine period

In BTM, the idea is to use same slope value for some adjacent points. Thus, the x axis is divided into 2^b equal intervals where $b < a$. The same slope value is used for the 2^{a-b}adjacent points in each 2^binterval. The TO size is calculated as

$$\mathrm{TO_{size}} = (\mathrm{R} - \mathrm{a}) \times 2^{\mathrm{b+c}} \tag{5}$$

where $2^c$is the number of offset value for each initial value. Fig. 4 gives the approximated $sin(x)$ where 0≤x≤π/2with BTM. The function is evaluated as

$$\mathrm{f_{app}(x) = TIV(x) + TO(x)} \tag{6}$$

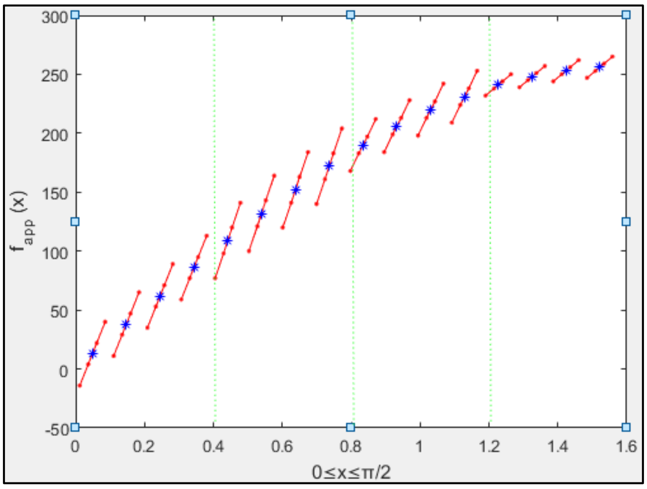


Figure 4. Approximated sine using BTM with R=8, a=4, b=2, c=2

As previously mentioned, LUT stage of a DDFS converts the phase value from the phase accumulator to amplitude values. To do this, it uses the P bit phase information as the address counter of both the TIV and the TO. First a bits of the word is used for the TIV, and the rest c bits and the most significant b bits of the word is also used for the TO. The decomposition of phase the word is given in Fig. 5.

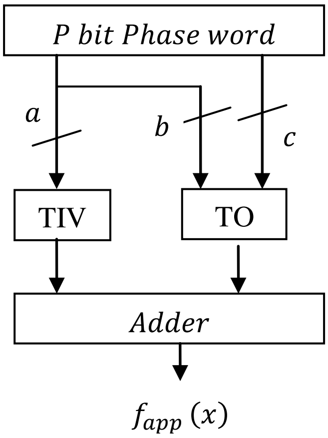


Figure 5. Phase word decomposition

3. Design

Inthisstudy, BTM wasusedtogetherwiththequadrantcompressiontechniquewhichusesthe sine symmetry. Inthistechnique, onlyonefourth of a sine sampledata is stored in thetables, andthe rest of thefunction is generatedbyusingthesevalues.

3.1. Phase Accumulator

A 32 bitscounter is created as thephaseaccumulator. Thecountercountswitheveryrisingedge of theclocksignalupto 2^N. FTW, the step size of thecounter, changestheoutputfrequency of the DDFS. The 32 bitscountervalue is truncatedto 20 bits. Themostsignificant 2 bitsof these data isusedtogeneratethehiddenquarters of the sine values, andthe rest representsthe 18 bitsphaseword. Theblockscheme of thecounter is given in Fig. 6.

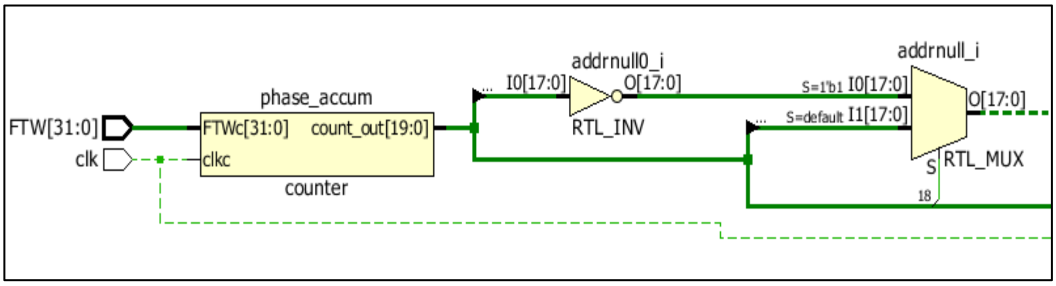
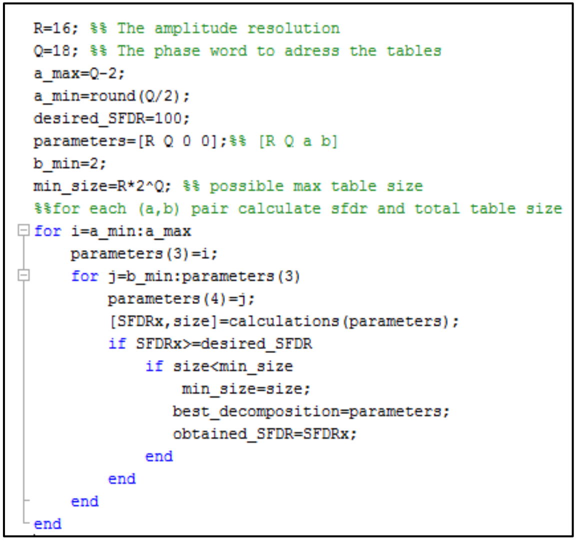


Figure 6. Block scheme of the counter

3.2. Best Decomposition of the Phase Word

Thegoal is todesign a DDFS with 18 bitsphaseand 16 bitsamplituderesolutionand a SFDR levelover 100 dB. An algorithm is createdtofindoutbestdecomposition of thephasewordtoobtainthetarget SFDR withthe minimum size of therequiredmemory. TheMatlabcode of thealgorithm is given in Fig. 7. Byusingthealgorithm, theparameters a, b and c arefound as 10, 3 and 8, respectively.



```
R=16; %% The amplitude resolution
Q=18; %% The phase word to adress the tables
a_max=Q-2;
a_min=round(Q/2);
desired_SFDR=100;
parameters=[R Q 0 0];%% [R Q a b]
b_min=2;
min_size=R*2^Q; %% possible max table size
%%for each (a,b) pair calculate sfdr and total table size
for i=a_min:a_max
    parameters(3)=i;
    for j=b_min:parameters(3)
        parameters(4)=j;
        [SFDRx,size]=calculations(parameters);
        if SFDRx>=desired_SFDR
            if size<min_size
                 min_size=size;
                best_decomposition=parameters;
                obtained_SFDR=SFDRx;
            end
        end
    end
end
```

Figure 7.Matlab code of the best decomposition algorithm

3.3. LUTs (Phase to Amplitude Conversion)

As thephasetoamplitudeconversionstage, twoBlockRandom Access Memories (BRAMs) areused. Thedimensions of thetablesaredetermined as 16×2^{10}and 6×2^{11}withtheequations (2) and (5). Theblockscheme of thephasetoamplitudepart is given in Fig. 8. Thecontents of thetablesareevaluatedbyusing a MATLAB code. Thecode is given in Fig. 9.

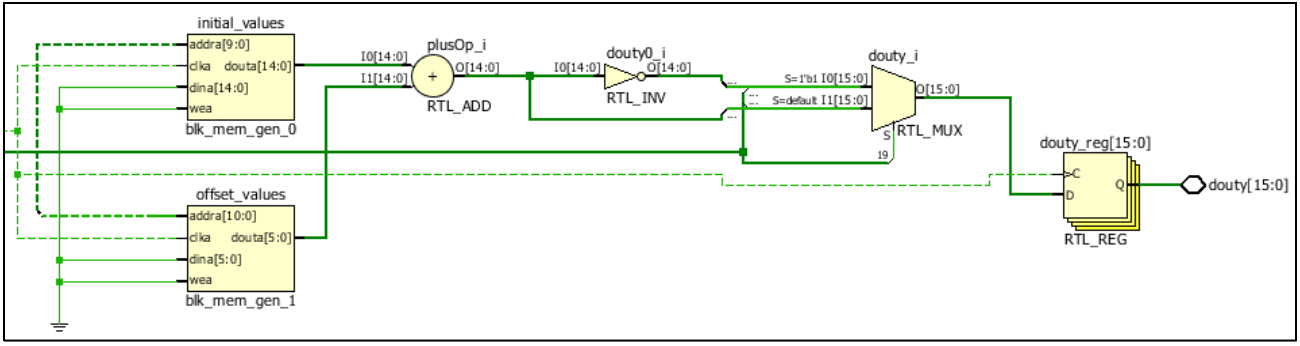
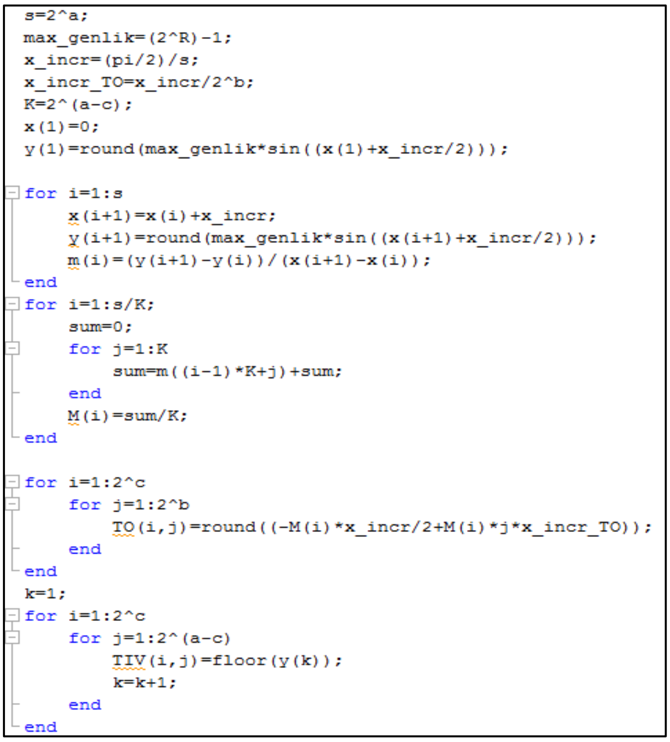


Figure 8. Block scheme of the phase to amplitude conversion stage



```
s=2^a;
max_genlik=(2^R)-1;
x_incr=(pi/2)/s;
x_incr_TO=x_incr/2^b;
K=2^(a-c);
x(1)=0;
y(1)=round(max_genlik*sin((x(1)+x_incr/2)));

for i=1:s
    x(i+1)=x(i)+x_incr;
    y(i+1)=round(max_genlik*sin((x(i+1)+x_incr/2)));
    m(i)=(y(i+1)-y(i))/(x(i+1)-x(i));
end
for i=1:s/K;
    sum=0;
    for j=1:K
        sum=m((i-1)*K+j)+sum;
    end
    M(i)=sum/K;
end

for i=1:2^c
    for j=1:2^b
        TO(i,j)=round((-M(i)*x_incr/2+M(i)*j*x_incr_TO));
    end
end
k=1;
for i=1:2^c
    for j=1:2^(a-c)
        TIV(i,j)=floor(y(k));
        k=k+1;
    end
end
```

Figure 9. MATLAB code to evaluate the LUT contents

4. SimulationResults

Thecreateddesign is simulated in VIVADO 2016.3 software. Thedesign is testedunder 100 MHz and 400 MHz referenceclockinput. Theoutputfrequency is adjustedtovariousfrequenciesbetween 23 mHz and 30 MHz. FTW is calculatedby (1). Table 2givessome FTW valuesforsomefrequencies.

Table 2. FTW values for some frequencies

f_{clk}	FTW		f_{out}	T_{out}
	Decimal	hex		
100 MHz	1	1	23 mHz	43.48 s
	43	2B	1 Hz	1 s
	42950	A7C6	1 kHz	1 ms
	42949673	28F5C29	1 MHz	1 µs
	214748365	CCCCCCD	5 MHz	200 ns
400 MHz	107374182	6666666	10 MHz	100 ns
	214748365	CCCCCCD	20 MHz	50 ns
	322122547	13333333	30 MHz	33.3 ns

Theoutputsignal is named as douty in thedesign. Thesignal has 4.5clockdelaywhich is 45 nsfor 100MHz inputand 11.25 nsfor 400 MHz input. Theinputclock has 1 µs delay. Thus, theperiod of the*douty* is showedbetweentwomarkers. Theblueone is thestart of thesignalandfixed at 1045 ns. Theyellowone is theend of thesignalandfixed at thelastdigitalvalue of thedoutyforoneperiod. ThefiguresFig.10toFig.16 showthattheperiod of thedouty is exactlysamewiththecalculations.

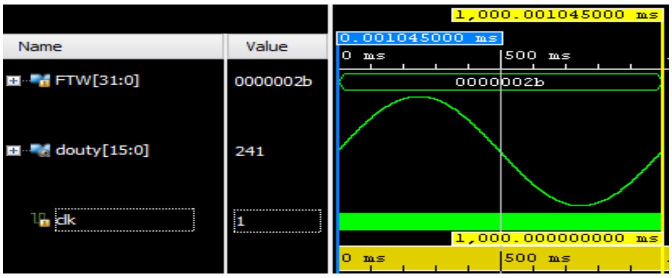


Figure 10. The Generated 1 Hz sine wave (clk =100 MHz)

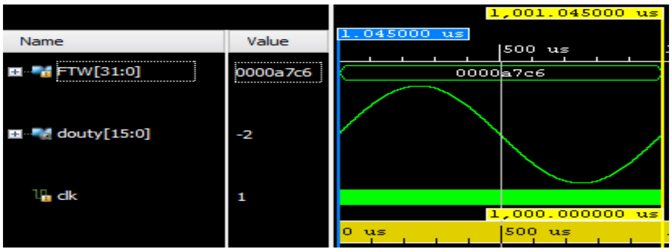


Figure 11. The Generated 1 kHz sine wave (clk =100 MHz)

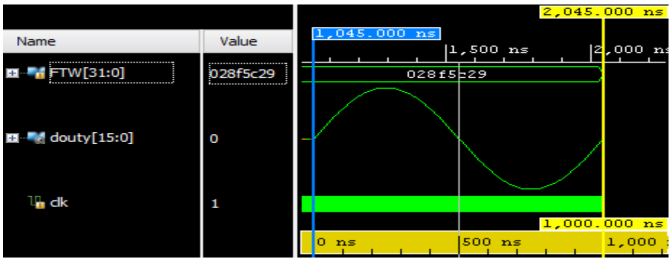


Figure 12. The Generated 1 MHz sine wave (clk =100 MHz)

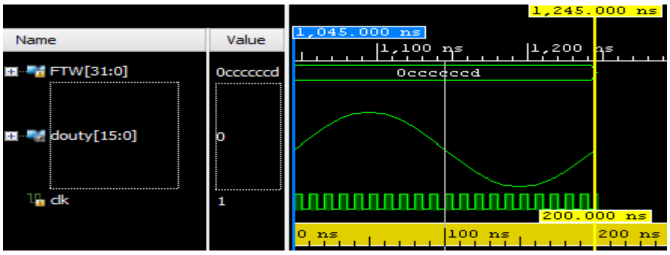


Figure 13. The Generated 5 MHz sine wave (clk =100 MHz)

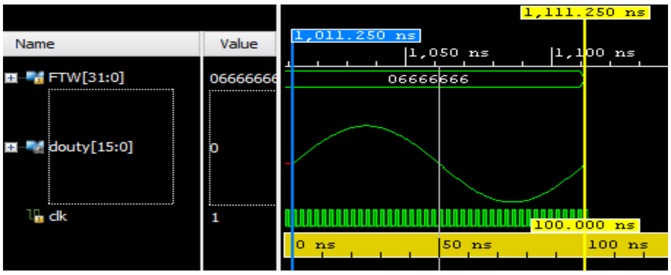
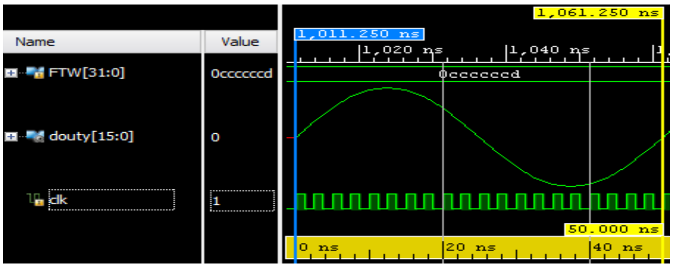
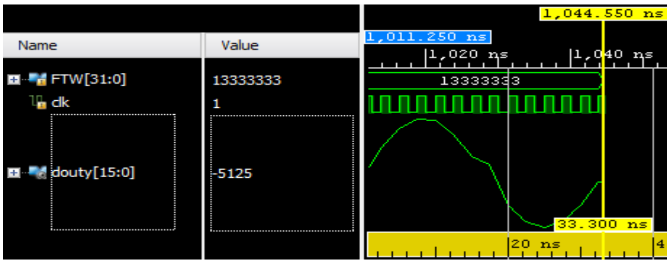


Figure 14. The Generated 10 MHz sine wave (clk =400 MHz)



Name	Value
FTW[31:0]	0cccccccd
douty[15:0]	0
clk	1

Figure 15. The Generated 20 MHz sine wave (clk =400 MHz)



Name	Value
FTW[31:0]	13333333
clk	1
douty[15:0]	-5125

Figure 16. The Generated 30 MHz sine wave (clk =400 MHz)

5. Conclusion

A LUT based DDFS design has beenproposed in thisstudy. Bipartitetablemethodandquadraticcompressionmethodareusedtogethertolessenthe LUT size. Firstly, the DDFS is brieflyintroducedand BTM is handled. Later on, thedetails of thedesign is focused, blockschemesandrelatedcodesaregiven. Finally, simulationresults of thedesignareshared.

Thedesignprovides 100 dB SFDR levelwiththeLUTswhose size are$16 \times 2^{10}$and 6×2^{11} , respectively. 32 bit phaseand 16 bit amplituderesolutionarealsoprovided. Byusing BTM andquadraticcompressionmethod, the LUT size is lessen 585 timesthan a traditional DDFS whichprovidesthesame SFDR andresolutionvalues. Thedesign is testedwith 100 MHz and 400 MHz inputclocks. Theoutputfrequency is adjustedbetween 23 mHz and 30 MHz. Noticeabledistortionsareobservedfor 30 MHz andhigherfrequencies.

Acknowledgements

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References

[1] C.Nie, X.Wang, H.Zhao, “W-band Transceiver Design of FMCW Radar with High Resolution”, *5th IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications*, 2013, pp. 691-693.

[2] A. Al Safi, B. Bazuin, “FPGA Based Implementation of BPSK and QPSK Modulators Using Address Reverse Accumulators”, *IEEE 7th Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON),* 2016, pp. 1-6.

[3] D. Sarriá, O. Pallarés, J. del-Río Fernández, A. Mànuel-Làzaro, “Low Cost OFDM Based Transmitter for Underwater Acoustic Communication”, *MTS/IEEE OCEANS, Bergen,* 2013, pp. 1-4.

[4] S. Yunxia, C. Bingyan, Z. Juan, T. Yingying, G. Yuan and S. Minglei, “Design of Time-Delay Detection Equipment for Signal Circuit”, *12th International Conference on Electronic Measurement & Instruments,* 2015, pp. 824-830.

[5] C. Lv, D. Fan, B. Shi, W. Wang and Z. Liu, “A Distortion Tester of Geophone Based on FPGA”, *IEEE International Conference on Automation and Logistics (ICAL),* 2009, pp. 1289-1092.

[6] X. Cheng, H. Zhao, Y. Dai and X. Liu, “Image Acquisition Design of the AOTF Imaging Spectrometer Based on SOPC”, *International SoC Design Conference (ISOCC),* 2011, pp. 266-269.

[7] K. Peng ,X. Liu and P. Huang, “Study on The Wireless Energy Supply System in The Implantable Cardiac Pacemaker”, *6thInternational Conference on Intelligent Systems Design and Engineering Applications (ISDEA),* 2015, pp. 778-781.

[8] R. Storch and T. Musch, “Synthesis Concepts of Signals With High Spectral Purity for the Use in Impulse Radar Systems”, *IEEE Transactions on Instrumentation and Measurement,* vol. 64, pp. 2574-2582, Sept. 2015.

[9] S. Thuries, E. Tournierand J. Graffeuil, “A 3-bits DDS Oriented Low Power Consumption 15 GHz Phase Accumulator in a 0.25 µmBiCMOSSiGe:C Technology”, *13th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* 2006,pp. 991-994.

[10] H. Jafari, A. Ayatollahi, and S. Mirzakuchaki, ” A Low Power, High SFDR, ROM-less Direct Digital Frequency Synthesizer”, IEEE Conference on Electron Devices and Solid-State Circuits, 2005, 829-832.

[11] S. Yanbin, G. Jian and C. Ning, “High Precision Digital Frequency Signal Source Based on FPGA”, *International Conference on Solid State Devices and Materials Science*, 2012, pp. 1342-1347.

[12] F. Dinechin and A. Tisserand,“Multipartite Table Methods”, *IEEE Transactions On Computers*, vol.54, pp. 319-330, Mar. 2005.

[13] A. G. M. Strollo, D. De Caro and N. Petra, “A 630 MHz, 76 mW Direct Digital Frequency Synthesizer Using Enhanced ROM Compression Technique”, *IEEE Journal of Solid-State Circuits*, vol.42, pp. 350–360, Feb. 2007.

[14] D. De Caro, N. Petra, and A. G. M. Strollo, “Reducing Lookup-Table Size in Direct Digital Frequency Synthesizers Using Optimized Multipartite Table Method”, *IEEE Transactions On Circuits And Systems*, vol.55, pp. 2116-2127, Aug. 2008.

[15] T. Menakadevi and M. Madheswaran, “Direct Digital Synthesizer using Pipelined CORDIC Algorithm for Software Defined Radio”, *International Journal of Science and Technology*, vol. 2, pp.372-378, June 2012.

[16] Y.H. Chen and Y. A. Chau, “A Direct Digital Frequency Synthesizer Based on a New Form of Polynomial Approximations”, *IEEE Transactions on Consumer Electronics*, vol.56, pp. 436-440, May. 2010.

[17] Y. Song and B. Kim,“A 14-b Direct Digital Frequency Synthesizer With Sigma-Delta Noise Shaping,”, *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 847–851, May 2004.